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ESTIMATION OF STATIC AND DYNAMIC PARAMETERS OF FLASH ADC USING 180 NM TECHNOLOGY

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Abstract—This paper presents the design of Analog to Digital Convertor (ADC). For ADC there are mainly four different methods, Flash ADC, Pipelined ADC, Successive Approximation ADC, Sigma Delta ADC. The Flash ADC is the Fast ADC. For Designing the ADC, the design issues are important. The design issues which consist first CMOS inverter used in CDC architecture, MUX based Decoder. The parameters important are Static and Dynamic. In static parameters Differential Non Linearity Error (DNLE), Integral Non Linearity Error (INLE) and in dynamic parameters Signal to Noise Ratio (SNR), Effective Number of Bits (EONB), Spurious-Free Dynamic Range (SFDR), Dynamic Range (DR).In this papers, the design and the results are with the help of Tanner Tool 13 software.

Keywords — ADC, DNLE, INLE, SNR, EONB, SFDR, DR, CDC, Mux based Decode, Tanner Tool 13.

I. INTRODUCTION

Analog to digital convertor circuit converts analog signal into digital signal. Analog signal is the signal whose amplitude is continuously changing with respect to time But in the Digital signal the amplitude and time is discrete. The ADC is characterized by three factor speed, area, and power consumption, the cost of ADC is varying from application to application.

To increase the speed of ADC, design the ADC with small voltage supply and shrink the size of ADC, for this application we are designing Flash ADC with Clocked Digital Convertor (CDC) configuration which eliminates the resistive network required for generation of internal reference voltage using Tanner tool 13 Software.

1.1 Types of ADC

- Sigma Delta ADC.
- Successive Approximation Register (SAR) ADC.
- Pipelined ADC.
- Flash ADC.

Comparison Plot between different ADC

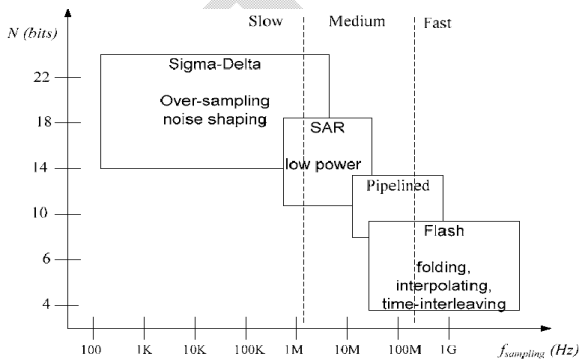

Fig 1 : Comparison of different ADC[9]

1.2 Design Issues

- Clocked Digital Comparator
- Transistor Inverter Quantizer (TIQ)
- CMOS Inverter as Phase Shifter
- CMOS Inverter as Quantizer
- Transmission Gate
- Multiplexer Based Decoder

Clocked Digital Comparator [8]

For conversion of analog signal into digital signal requires the Quantizer, sampler and encoder. In clocked digital comparator shown in Fig. 2, the first stage consists of two inverter. The first inverter is acts as the Quantizer by settling the comparator voltages for comparison and the second inverter is acts as the logic level inversion. In ADC structure the output should be same as the input signal but the first inverter inverts the input therefore the output is out of phase so for nullifying the phase shift we have to add the second inverter. This CDC consists of two parts. First part is Transistor Invertor Quantizer (TIQ) and Transmission Gate (TG).

Transistor Inverter Quantizer (TIQ) [8]

Comparator structure is most important part in Flash ADC architecture. The role of comparator is to compare the input

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signal with reference voltage and gives the respective logic levels (1 and 0).

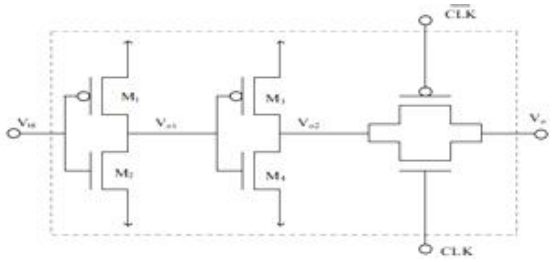

Fig 2 : Clocked Digital Comparator [8]

The comparator converts the input signal into only two logics (logic1 and logic 0) depending on the values of input. If the values of input is greater than threshold value then it will give logic 1 otherwise it will give logic 0.

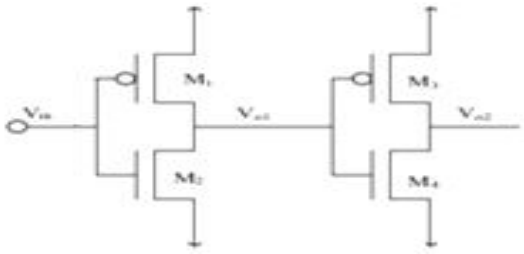

Fig 3 : Transistor Inverter Quantizer [8]

The TIQ shown in fig 3 is the first stage of CDC, it is use for generating the internal reference voltage which is required for comparison. The internal reference voltage is generated using number of methods like resistive ladder network, systematically varying the size of transistor. In TIQ the internal reference voltage is generated by systematic varying the width of NMOS and PMOS. We are keeping the length of transistor is same because the length of transistor is depend on the technology.

CMOS Inverter as Phase Shifter [8]

The inverter provides phase shift, amplification, quantization stages. Let us consider the signal given to the clocked digital comparator is sine wave then inverter gives the output negative of sine wave, x(t)=A*sin(wt) as input inverter gives $x_1(t)$=A*sin(wt+pi) further solved this equation by applying some mathematical relationship

sin(A+B) = sinA*cosB+cosA*sinB

$x_1(t)$= A*sin(wt)*cos(pi)+A*cos(wt)*sin(pi)

$x_1(t)$= - A*sin(wt)

[As cos(pi)=-1 and sin(pi)=0]

CMOS Inverter as Quantizer [9]

The Clocked Digital Comparator compares the input voltage with reference voltage generated by varying the width of each comparator depending on the value of reference voltage each comparator gives its logic level. The four bit comparator requires fifteen comparators since they will generate their respective fifteen levels in this way they are acting as Quantizer.

Transmission Gate [8]

The second stage consists of transmission gate. The use of transmission gate is for sampling the signal. As we know the transmission gate work on clock signal if the transmission gate is positive edge enabled clocked then it works only for positive edges that means it only pass the logic for positive edge and blocked the logic for negative edge that's why we generally called transmission gate as the switch.

The frequency on which clocked operates called as sampling frequency and the sampling frequency should be more than twice of input frequency, so the clocked digital comparator is acting as the Quantizer and sampler. It can be shown that the *Vm* point on the VTC of a CMOS inverter, which is shown in Fig. 4, can approximately be given by the following equation

$$V_m = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}(V_{dd} - |V_{Tp}|) + V_{Tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}$$

Fig 4 : Formula for Finding Internal Reference Voltage [8]

Where V_{Tp} and V_{Tn} are threshold voltages of PMOS and NMOS devices, *Wp* and *Wn* are widths of PMOS and NMOS, μp and μn are hole mobility and electron mobility respectively.

CDC Design using Tanner Tool 13

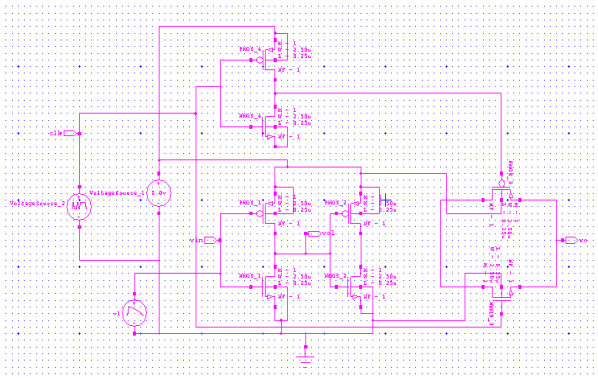

Fig 5 : Schematic of CDC

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CDC Simulation

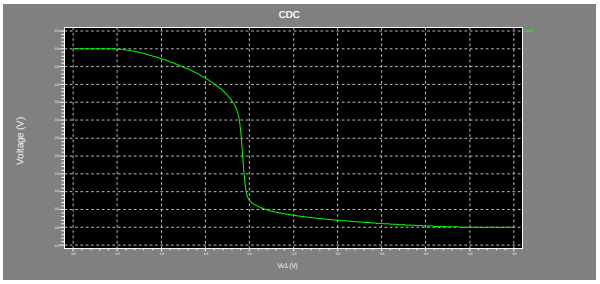

Fig 6 : Waveform of CDC

No. of Comparators can be calculated by the formula = $2^n - 1$

For 4 bits ADC, Put n = 4, No. of CDC required = 15

Design of 15 CDCs

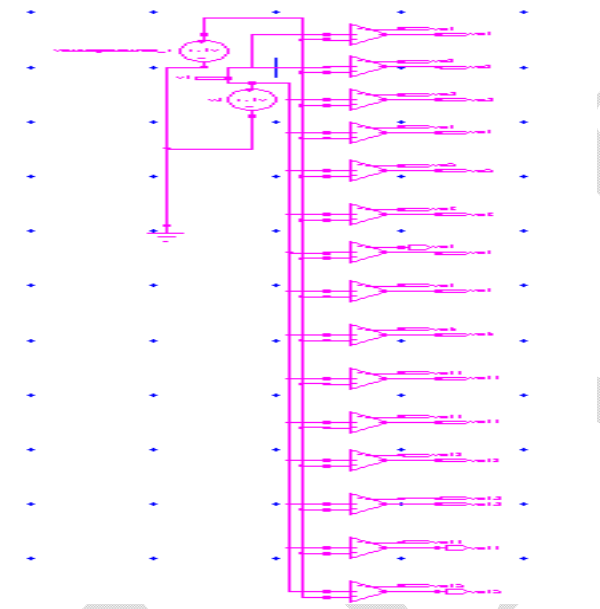

Fig 7 : Schematic of 15 CDC's

15 CDC Simulations

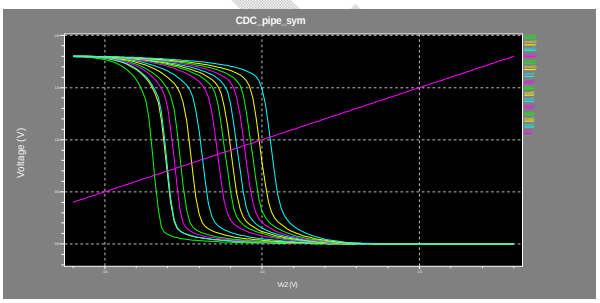

Fig 8 : Waveforms of 15 CDC's

Multiplexer Based Decoder [6]

The multiplexer based decoder circuit uses 2:1 Mux so we required 11 Mux for implementing 15 inputs. The 2:1 Mux required two input signals with one select line, the select line should vary between two logics 0 to 1 depending on the select line the Mux'll transmit the logic, the truth table of 3 bit thermometer code itself expressing the logic the M.S.B. bit of binary input equal to middle bit of thermometer code because it follows the twin logic.

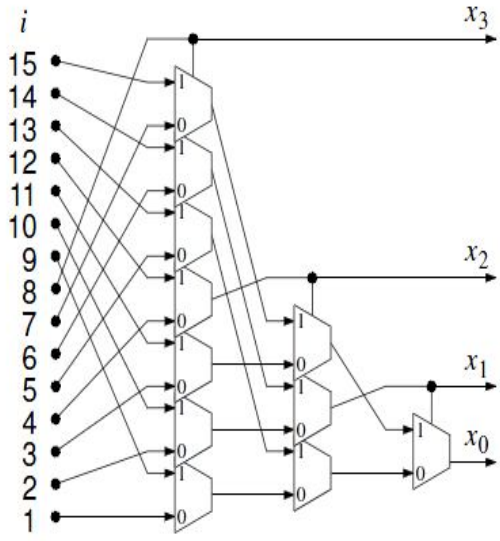

Fig 9 : Multiplexer Based Decoder [6]

The working principal of multiplexer based decoder is shown in table 1, the M.S.B bit of the output is equal to the T_2 bit of input (Middle bit) and L.S.B. of output is equal to the value of T_1 and T_2 respectively. In this design 11 multiplexer are used because in first stage there are 15 inputs for implementing 15 input 7 mux are used in the second stage 3 mux are used the output of middle multiplexer is acting as select line in the second stage while in last stage 1 mux is required.

Table 1: conversion of 3-bit thermometer code to binary code [6]

Thermometer code			Binary Code	
T_3	T_2	T_1	B_2(MSB)	B_1
0	0	0	0	0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1

Design of Multiplexer Based Decoder using Tanner Tool 13

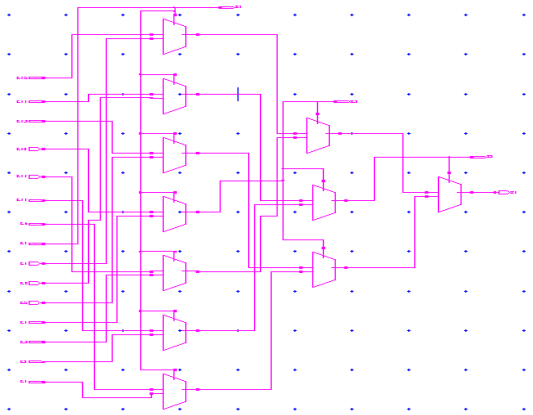

Fig 10: Schematic of Multiplexer Based Decoder.

Interconnection of CDC and Multiplexer Based Decoder to make it as ADC

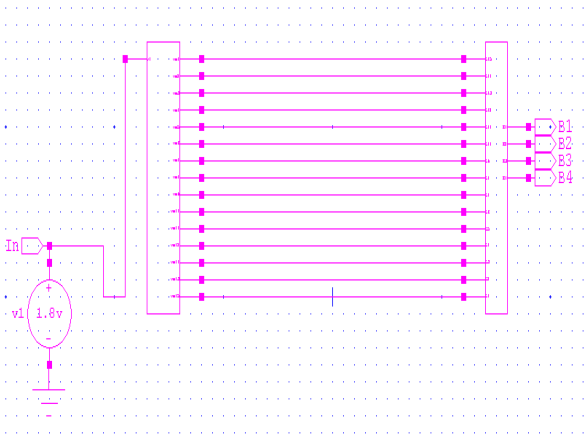

Fig11 : Schematic of ADC

Output of ADC

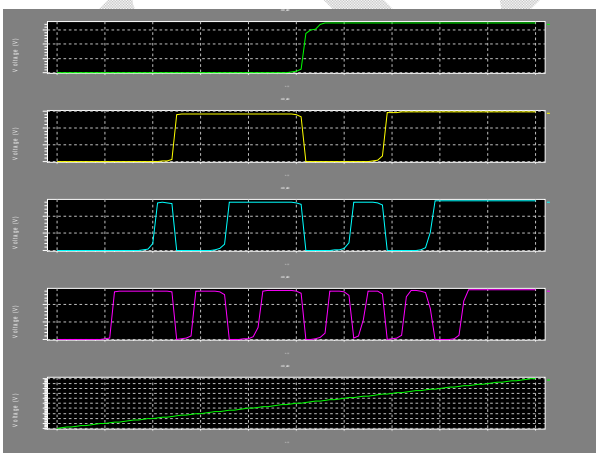

Fig 12: Output Waveforms of ADC

Table 2 - For Different V(M)

Sr. No.	INTERNAL REFERANCE VOLTAGE V(m)	W(p) in um	W(n) in um
1	0.588	1.58	0.23
2	0.624	1.38	0.25
3	0.638	1.23	0.27
4	0.653	1.1	0.29
5	0.675	0.95	0.31
6	0.707	0.88	0.51
7	0.728	0.82	0.71
8	0.744	0.74	0.9
9	0.776	0.68	1.12
10	0.805	0.6	1.37
11	0.886	0.5	1.52
12	0.899	0.42	1.78
13	0.907	0.34	2.04
14	0.925	0.24	2.13
15	0.943	0.16	2.56

Static Parameter

The static parameters describe the errors between the actual points and the ideal points in the staircase transfer function of an ADC when it is converting DC signals. Figure shows the staircase transfer function of an ADC. The actual characteristic does not match with the ideal characteristic in both the reference voltage and the width of horizontal steps, as shown in Figure. These differences are essentially due to differential non-linearity error (DNL), and integral non-linearity error (INL).

Differential Non Linearity error

The Differential Non-Linearity error is calculated as its measures Horizontal change from ideal value of ADC. The DNL of the ADC should be as small as possible because it'll give you the missing code.

Integral Non Linearity error

The Integral Non-Linearity error is calculated as its measures Vertical change from ideal value of ADC. INL of the ADC

should be as small as possible because it'll give you the missing code.

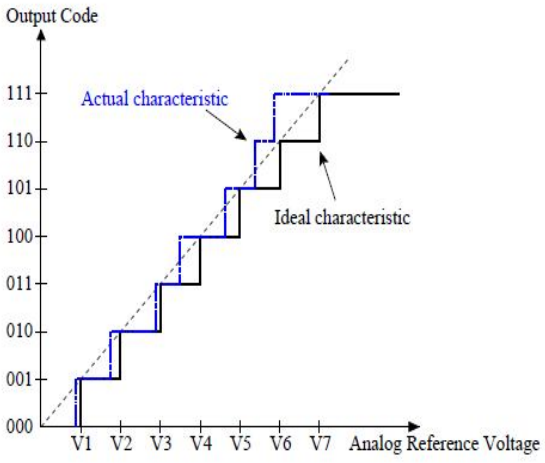

Fig 13: Staircase transfer function of ADC [9]

Table 3: for INL (Integral Non linear Error) and DNL (Differential Non linear Error) CALCULATION

Sr. No.	Actual Value (LSB)	Ideal Value (1LSB =0.588)	DNL=Actual Value-Ideal Value	INL
1	0.588	0.588	0	0
2	0.624	0.6133	0.0107	-0.01721
3	0.638	0.6386	-0.0006	0
4	0.653	0.6639	-0.0109	0.01143
5	0.675	0.6892	-0.0142	0.0183
6	0.707	0.7145	-0.0075	0
7	0.728	0.7398	-0.0118	0.017
8	0.744	0.7651	-0.0211	0.0264
9	0.776	0.7904	-0.0144	0.0224
10	0.805	0.8157	-0.0107	0.0155
11	0.886	0.841	0.045	-0.0752
12	0.899	0.8663	0.0327	-0.0642
13	0.907	0.8916	0.0154	-0.0454
14	0.925	0.9169	0.0081	-0.0358
15	0.943	0.9422	0.0008	0

Dynamic Parameters

For the dynamic parameters we required reconstructed original signal. For reconstruction we required DAC.

II. DIGITAL TO ANALOG CONVERTOR

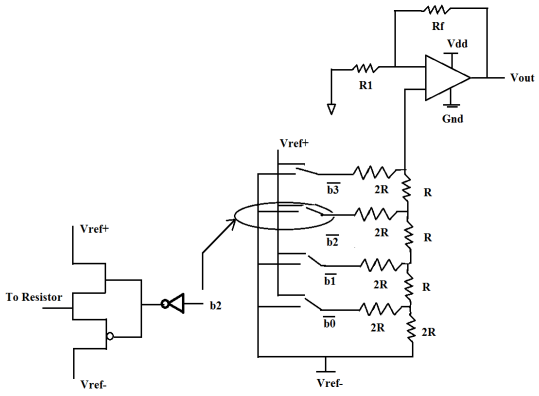

Figure 14: Circuit diagram of DAC Convertor.

DAC Design using Tanner Tool 13

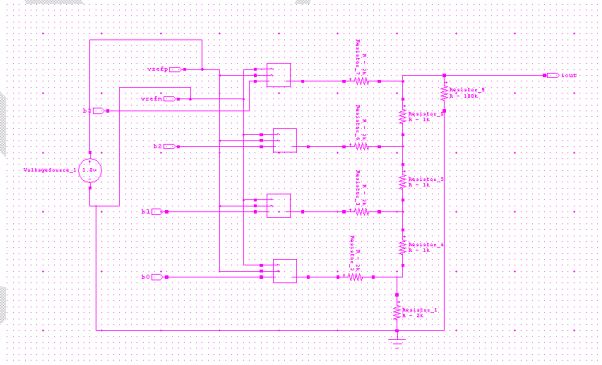

Fig15: DAC Design.

Interconnection of ADC DAC to RECONSTRUCT THE ORIGINAL SIGNAL

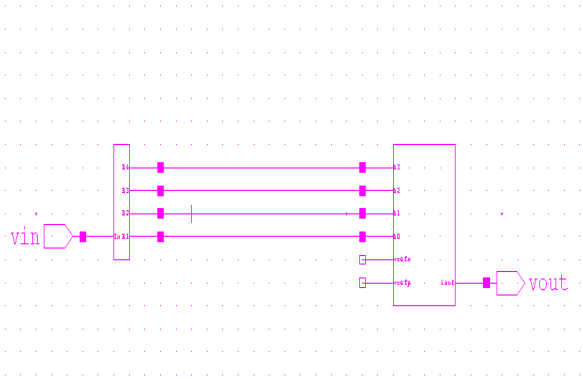

Fig 16 : Interconnection of ADC DAC Design.

Output of ADC-DAC

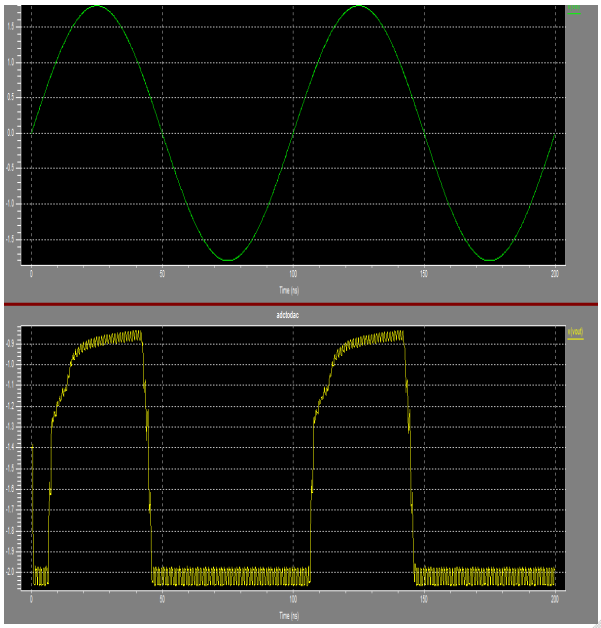

Fig 17 : Output of ADC DAC Design.

Output of ADC-DAC WITH FFT

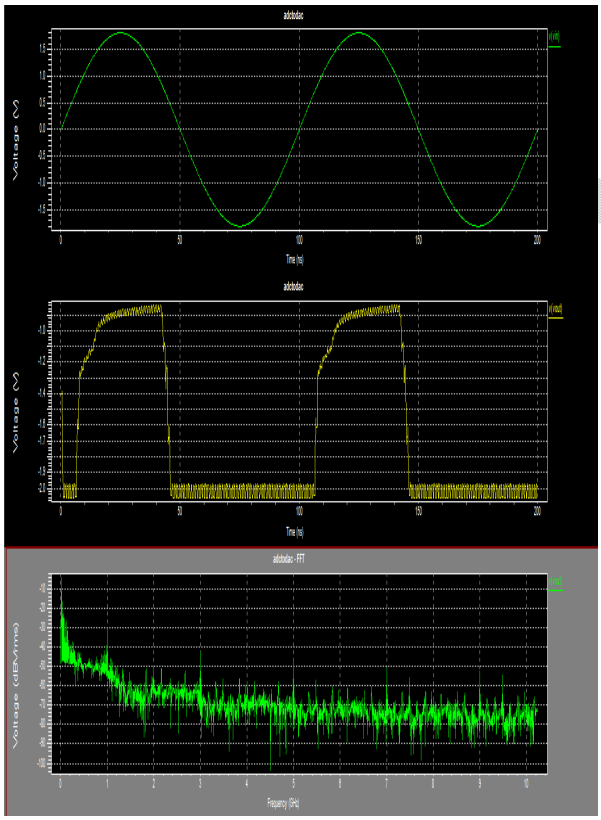

Fig 18 : Output of ADC DAC Design with FFT.

Table 4 for Results of ADC & DAC PARAMETERS

PARAMETERS	SPECIFICATION
ARCHITECURE	FLASH
RESOLUTION	4 BIT
POWER SUPPLY	1.8 V
TECHNOLOGY	180 nm
SAMPLING FREQUENCY	1 GHZ
INPUT FREQUENCY	10 MHZ
SNR	25.5 DB
SFDR	14 DB
ENOB	3.945 BIT
DR	23.5 DB
DNL	-0.0211/+0.045 LSB
INL	-0.0752/+0.0264 LSB
REFERENCE VOLTAGE RANGE	0.588/0.943

Table 5 for COMPARISON WITH STANDRED DESIGN

PARAMETERS	SPECIFICATION	IDEAL VALUE
ARCHITECURE	FLASH	FLASH
RESOLUTION	4 BIT	4 BIT
POWER SUPPLY	1.8 V	1.8 V
TECHNOLOGY	180 nm	180 nm
SAMPLING FREQUENCY	1 GHZ	1 GHZ
INPUT FREQUENCY	10 MHZ	10 MHZ
SNR	25.5 DB	25.84 DB
SFDR	14 DB	---------
ENOB	3.945 BIT	4 BIT

DR	23.5 DB	---------
DNL	-0.0211LSB / +0.045LSB	+0.5 LSB / -0.5 LSB
INL	-0.0752LSB / +0.026LSB	+0.5 LSB / -0.5 LSB
REFERENCE VOLTAGE RANGE	0.588 / 0.943	0.588 / 0.942

III. CONCLUSION

By considering this methodology of designing the 4 bit flash ADC with the Tanner tool 13 software, we can convert the analog input signal to the 4 bit digital output. Find all the static and dynamic parameters of 4 bit flash ADC and Compare these parameters with the standard parameters to get all the ideal parameters.

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